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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,573	11/05/2003	Norio Masui	244948US2	1050

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EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,573	MASUI, NORIO	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-14 and 17* is/are allowed.

6)☒ Claim(s) *1 and 16* is/are rejected.

7)☒ Claim(s) *2-7 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/700,573 filed on 11/05/2003.

2. Claims 1-17 have been submitted for examination.

3. Claims 1-17 have been examined.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 16 rejected under 35 U.S.C. 102(b) as being anticipated by Yeager, U.S. Patent 6,266,755.

7. With respect to claim 1, Yeager teaches of an address translation unit performing address translation from a virtual address to a physical address, comprising: a data entry part holding data of said physical address (fig. 4B; items 520, 521; column 9, lines 51-57); and

a tag entry part storing an address space identifier and virtual address as a tag of said data entry part (fig. 4b; items 510, 511; column 8, lines 51-59; column 9, lines 29-36; where the page address and region bits of the virtual address are stored in a register 510; where the ASID is stored in a register 511),

said tag entry part comprising: an address space identifier hold part holding said address space identifier (fig. 4b; item 511);

an address space identifier comparison judgment part comparing an address space identifier hold value held in said address space identifier hold part with an address space identifier input value to be inputted newly (fig. 4b; item 506; column 9, lines 29-36; where a comparator compares the current virtual address' ASID with the one stored in the register);

a virtual address hold part holding said virtual address (fig. 4b; item 510); and

a virtual address comparison judgment part comparing a virtual address hold value held in said virtual address hold part with a virtual address input value to be inputted newly (fig. 4b; item 505; column 8, lines 51-59; where a comparator compares the page address and region bits of the virtual address with those stored in the register 510),

said virtual address comparison judgment part having a charge circuit for charging its output line and a charge inhibit circuit for inhibiting charge to said output line (fig. 4b; column 9, lines 48-57; As the comparator outputs a high signal when a match occurs, it must have a circuit that charges the output to a high voltage. The other

output of the comparator must be a low value, there must be a circuit that grounds the comparator's output, thus keeping it from going high),

wherein a potential state of said output line is controlled based on the comparison result between said address space identifier hold value and said address space identifier input value, to determine execution or non-execution of comparison operation between said virtual address hold value and said virtual address input value at the time of address translation (fig. 4b; column 9, lines 29-36; where upon a match of comparator 506 (ASID values) enables the comparing of the virtual addresses. If a match does not occur and the global bit is not set, then the comparator is not enabled as the output of AND gate 577 is "0" and not "1" which is needed to enable the comparator).

8. With respect to claim 16, Yeager teaches of the limitations of the parent claim as discussed supra. Yeager also teaches of wherein said virtual address comparison judgment part compares said virtual address hold value with said virtual address input value at the time of address translation, when said address space identifier hold value matches said address space identifier input value, and does not compare said virtual address hold value with said virtual address input value at the time of address translation, when said address space identifier hold value mismatches said address space identifier input value (fig. 4b; column 9, lines 29-36; column 11, lines 35-40; where upon a match of comparator 506 (ASID values) enables the comparing of the virtual addresses. If a match does not occur and the global bit is not set, then the

comparator is not enabled as the output of AND gate 577 is "0" and not "1" which is needed to enable the comparator).

Allowable Subject Matter

9. Claims 8-14 and 17 are allowed.

10. Claims 2-7 and 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

a. With respect to claims 2-7 and 15, the prior art of McGrath et al. 6,604,187 teaches of the address space identifier hold part and the virtual address hold part implemented in a CAM (fig. 2; column 7, lines 55-66). The prior art of Yeager teaches of said virtual address comparison judgment part receives a comparison result signal obtained in said address space identifier comparison judgment part and performs a comparison at least between said virtual address hold value and said virtual address input value as previously cited. The combination of Yeager and McGrath also teaches of the connections cited in the claim (Yeager, fig. 4b). The prior art fails to teach of the virtual address comparator maintaining the output of the ASID comparator in a "floating state" when the ASID values match. In other words, the output from the ASID comparator feeds directly into the virtual address comparator and the virtual address comparator does not do anything to

that output value, and outputs that ***same*** value, i.e. there is no interaction between the ASID output value and the virtual address comparator.

b. With respect to claims 8-14 and 17, the prior art of Yeager teaches of all the limitations of claim 1 included in claim 8 as cited above. Yeager also teaches of a valid bit holding information as to whether data of said tag entry part is valid, and wherein said virtual address comparison judgment part determining execution or non-execution of comparison operation between said virtual address hold value and said virtual address input value at the time of address translation, based on the comparison result between said address space identifier hold value and said address space identifier input value, and said information as to whether data of said tag entry part is valid or invalid (Yeager fig. 4b; column 11, lines 35-46). The prior art fails to teach of comparing a valid bit of the entry with a valid bit that is inputted with the desired virtual address to be translated as taught in independent claim 8.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER